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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/523,572	03/10/2000	Pascal Moniot	859063.463	5868

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EXAMINER	
SWICKHAMER, CHRISTOPHER M	
ART UNIT	**PAPER NUMBER**
2697	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/523,572	Applicant(s) MONIOT, PASCAL	
	Examiner Christopher M Swickhamer	Art Unit 2697	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-17* is/are rejected.

7)☒ Claim(s) *5,6 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. The claims are objected to because they include reference characters that are not enclosed within parentheses.

- Reference characters corresponding to elements recited in the detailed description of the drawings and used in conjunction with the recitation of the same element or group of elements in the claims should be enclosed within parentheses so as to avoid confusion with other numbers or characters which may appear in the claims. See MPEP § 608.01(m).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Claim 1 recites the limitation "the read mode" in line 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 7-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Shtayer (USP 5,414,701). Referring to Claim 1, Shtayer discloses a device for associating indexes to addresses chosen from among a greater number of values than the number of available indexes, including: tables (a memory) containing VPI's (indexes) and VP Pointers (respective check words) corresponding to predetermined bits of the addresses associated with the indexes (Fig. 3, col. 2, lns. 20-43, col. 5, lns. 30-col. 6, lns. 5); compressing (a packing circuit receiving) a current address and suppressing in this address bits determined by a pattern such that the suppressed bits correspond to bits of the VP Mask (check words), the packed address (provided by the packing circuit) being used to select in the read mode a table location (memory location); and (a comparator) indicating that the current address corresponds to the selected table location (memory location) if the bits of the VP Offset (check word) of the selected location are valid (equal to the) corresponding to bits of the current address (col. 6, lns. 19-50).

- Referring to Claim 2, Shtayer discloses the device of claim 1, wherein the device includes a mask (circuit) which, according to a predetermined mask, annuls bits other than those which are compressed (suppressed by the packing circuit), which also correspond to VP mask (check word) bits (col. 5, lns. 53-68).

- Referring to Claim 3, Shtayer discloses the device of claim 1, wherein each table (memory) location contains an enable bit indicating whether the location is occupied or not (col. 5, lns. 38-43).

- Referring to Claim 4, Shtayer discloses the device of claim 1, wherein the addresses are ATM network addresses, and the indexes identify connections of the device to one or several ATM networks (col. 4, lns. 40-51).

- Referring to Claim 7, Shtayer discloses an address association device, comprising: a mask (masking circuit) configured to receive a plurality of address bits and mask the address bits in accordance with a predetermined mask pattern (col. 5, lns. 50-56); a compressing operation (packing circuit) configured to receive address bits from the mask (masking circuit) and to a reduce the number of address bits to a Virtual Path Identifier (VPI, plurality of index bits) and a VP Mask (plurality of check word bits) according to a predetermined packing pattern (Fig. 3, col. 5, lns. 60-68); a table (memory) configured to receive from the packing circuit the VP Index (plurality of index bits) and the VP Pointer (plurality of check word bits) and to associate the received VP Index (index bits) and VP Pointer (check word bits) with the table (memory) location of a network connection (Fig. 3, col. 5, lns. 34-col. 6, lns. 18); and (a comparator) coupled to the table (memory) and configured to receive the plurality of address bits and to indicate if selected bits from the plurality of address bits correspond to a valid Virtual Path (the plurality of check word bits) associated with the table (memory) location addressed in the plurality of address bits (col. 6, lns. 19-50).

- Referring to Claim 8, Shtayer discloses the device of claim 7 wherein the mask (masking circuit) is configured by the predetermined mask pattern to mask bits not compressed (suppressed by the packing circuit) when the number of bits used to address a network connection in memory is fewer than the number of bits remaining after the plurality of address bits are compressed (reduced by the packing circuit, col. 5, lns. 60-65, col. 6, lns. 6-19).

- Referring to Claim 9, Shtayer discloses the device of claim 7 wherein each network connection in the table (memory) includes a Virtual Path Valid (VPV, enable) bit that is configured to signal when the network connection in the table (memory) is an active connection to the network (col. 6, lns. 5-50).

- Referring to Claim 10, Shtayer discloses the device of claim 9, further comprising a logic circuit coupled to the enable bit and to the comparator and configured to indicate if a selected location addressed by the plurality of address bits is an active location (col. 5, lns. 35-45).

- Referring to Claim 11, Shtayer discloses the circuit of claim 7, further comprising a register configured to store a base address corresponding to a beginning address in memory and, further comprising an adder for adding the base address to the index (plurality of address bits reduced by the packing circuit, col. 5, lns. 13-32).

- Referring to Claim 12, Shtayer discloses a method for associating addresses to memory locations, comprising: receiving a plurality of address bits and masking the address bits in. accordance with a predetermined mask pattern (col. 5, lns. 60-68); compressing (packing the masked plurality of) the address bits to reduce the number of address bits to a VP Index (a plurality of index bits) with a VP Pointer (check word bits) according to a predetermined packing pattern (Fig. 3, col. 5, lns. 33-68); associating the VP Index (plurality of index bits) and VP Pointer (check word bits) with a table (memory) location corresponding to a network connection; and to comparing selected bits from the plurality of address bits for a selected table (memory) location with selected bits associated with a table (memory) location addressed in the plurality of address bits and indicating if the connection is valid (there is a match, col. 6, lns. 6-50).

- Referring to Claim 13, Shtayer discloses the method of claim 12 wherein masking comprises configuring the predetermined masking pattern to mask bits not suppressed by packing when the number of bits used to address a selected memory location is fewer than the bits remaining after packing (col. 5, lns. 60-68).

- Referring to Claim 14, Shtayer discloses the method of claim 12, further comprising having a Virtual Path Valid bit (ANDing an enable bit) with the results of the comparing to determine if a selected table (memory) location is an active connection (col. 6, lns. 5-50).

- Referring to Claim 15, Shtayer discloses the method of claim 12 wherein packing comprises storing a base address corresponding to a beginning address in a table (memory) and adding the base address to the VP Pointer associated with the compressed VP Index (plurality of address bits reduced during packing, Fig. 3, col. 5, lns. 13-68).

- Referring to Claim 16, Shtayer discloses the method of claim 12 wherein compressing (packing) further comprises reducing the plurality of address bits to a compressed (packed) address comprising VP Index (a plurality of index bits) with an associated VP Pointer (check word bits) used to select a table (memory) location in a read mode (col. 5, lns. 13-68).

- Referring to Claim 17, Shtayer discloses the method of claim 14, further comprising disabling a Virtual Path Valid (enable) bit corresponding to a table (memory) location selected by the plurality of address bits (col. 6, lns. 5-20).

Allowable Subject Matter

5. Claims 5,6 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base

claim and any intervening claims. Claim 5 would be allowable over the prior art of record since the cited references taken individually or in combination fails to particularly disclose a device as stated in claim 4, wherein the addresses provided by the packing circuit have a 16-bit size, the indexes have a 10-bit size, and the check words correspond to the 20 most significant bits of the ATM addresses. It is noted that in the closest prior art of record, Shtayer (USP 5,414,701), shows a similar system for compressing ATM addresses using masks. Shtayer allows flexibility is choosing the bit size of the VP, VC, and Link table depending on the application. However Shtayer fails to give reasoning as to why the values of the applicant for the packing circuit, the index, and the check words should be chosen as claimed.

- Referring to Claim 18, Claim 18 would be allowable over the prior art of record since the cited references taken individually or in combination fails to particularly disclose a device configuring the predetermined mask pattern to mask bits to prevent accessing selected memory locations that have been previously addressed. It is noted that in the closest prior art of record, Shtayer (USP 5,414,701), shows a similar system for compressing ATM addresses using masks. However Shtayer fails to configure the masked pattern to prevent accessing memory locations that have been previously addressed.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Huang et al, USP 6,262,985, *Method and Apparatus for Full Range Translation of Large External Identifier to Small Internal Identifier.*

- Hoshino et al, USP 6,289,014. *Multiline-Correspondent Cell Header Conversion Apparatus and Method.*
- Kadambi et al, USP 6,335,932. *High Performance Self Balancing Low Cost Network Switching Architecture base on Distributed Hierarchical Shared Memory.*
- Joffe, USP 5,936,959. *Cell Routing in ATM Networks.*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M Swickhamer whose telephone number is (703) 306.4820. The examiner can normally be reached on 8:00-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (703) 305.4798. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308.9571 for regular communications and (703) 827.9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305.3900.

CMS
April 1, 2003

RICKY NGO
PRIMARY EXAMINER